MEMORY SYSTEM WITH DYNAMIC TIMING CORRECTION

TECHNICAL FIELD

The present invention relates to memory systems and memory devices, and more particularly, to dynamic timing correction in memory systems and memory devices.

BACKGROUND OF THE INVENTION

Timing of operations in synchronous memory systems must be tightly controlled if the memory system is to operate at optimum rates. Typically, timing of operations in synchronous systems is controlled by a memory controller operating in synchronization with edges of the master clock signal.

One problem that often occurs in such systems arises from differences in propagation times of signals between a memory controller and memory devices controlled by the memory controller. Such timing differences may prevent the memory system from operating at its optimum rate. For example, the memory controller typically accepts new data from a memory device at leading clock edges (*i.e.*, transitions of the master clock signal from low to high). If one of the memory devices outputs data at the specified clock edge, propagation delays from the memory device to the memory controller may cause the data to arrive later than the specified clock edge. Therefore, the memory device outputs data a short time before the leading edge to compensate for propagation of delays.

One problem with such an approach is that propagation delays between the memory device and memory controller will depend upon the effective distance between the memory controller and the memory device, which depends upon the routing of signal lines connecting the memory controller to the memory device. Consequently, the data may still not arrive at the memory

controller at the specified leading edge. Therefore, the memory controller must be prepared to accept the data for some time before and after the clock edge. To allow sufficient time to look for the data, the memory controller allots a larger than optimum time period for accepting the data. The overall speed of the memory system is limited correspondingly.

SUMMARY OF THE INVENTION

A memory system includes a memory controller coupled to a plurality of memory devices. The memory controller includes a master clock generator that provides a master clock signal for controlling timing of operations within the memory system. The memory controller also includes a data clock generator that provides a data clock signal to control timing of data transfer to and from the memory devices.

Each of the memory devices includes an echo clock generator that generates an echo clock signal in response to the master clock signal. The echo clock generator includes an output vernier that receives the master clock signal and produces a delayed data clock signal. The delayed data clock signal drives an output register to provide output data to a data bus. Each memory device also transmits the delayed data clock signal to the memory controller as the echo clock signal.

Within the memory controller a phase comparator compares the echo clock signal to the master clock signal to identify any phase shift of the echo clock signal relative to the master clock signal. In response to the determined phase shift, control logic of the memory controller provides control data to the memory devices to adjust the vernier, thereby reducing the phase shift.

In one embodiment, the phase comparator is formed from a plurality of phase detectors, where each phase detector has a first input driven by

the echo clock signal. The phase detectors also have second inputs that receive phase-shifted versions of the master clock signal.

To produce the phase-shifted versions of the master clock signal, the memory controller includes a delay-locked loop driven by the master clock signal. The delay-locked loop includes a multiple output variable delay circuit that outputs the phase-shifted versions of the master clock signal. In one embodiment, the phase-shifted versions of the master clock signal include versions shifted relative to the master clock signal by 0, $+\tau$, $-\tau$, $+2\tau$, and -2τ, where τ is a selected increment greater than half of the finest adjustment available in the vernier.

The use of a plurality of phase detectors driven by taps of a delay-locked loop allows the echo clock signal to be phase compared to the master clock signal in real time. Thus, the memory controller can dynamically adjust timing of the memory devices to accommodate drift in routing delays of the memory system.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a memory system including a memory controller and eight memory devices.

Figure 2 is a block diagram of one of the memory devices of Figure 1.

Figure 3 is a block diagram of another embodiment of the memory system including a memory controller and eight memory devices where each memory device includes an echo clock generator coupled to the memory controller and the memory controller includes a phase comparing circuitry.

Figure 4 is a block diagram of one of the memory devices of the memory system of Figure 3.

Figure 5 is a block diagram of the master controller of Figure 3.

Figure 6 is a block diagram of a computer system including the memory system of Figure 3.

DETAILED DESCRIPTION OF THE INVENTION

As shown in Figure 1, a memory system 40 includes a memory controller 42 that controls eight memory devices 44 as directed by a logic control circuit 43. The memory devices 44 and memory controller 42 operate according to a packet protocol. According to the packet protocol, the controller 42 generates a control data packet containing control data CDAT for reading to or writing from one of the memory devices 44 or for initiating a memory event, such as reset or autorefresh. Among the control data CDAT, the data packet includes fields identifying the memory device 44 to which the packet is directed, fields containing command data, and fields containing addressing information, such as row, column, bank, or register addresses. The memory controller 42 transmits the control data packet to all of the memory devices 44 on a control data bus 46 that is coupled to control data inputs of all of the memory devices 44.

In addition to the control data packets, the memory controller 42 also provides a master clock signal MCLK on a master clock bus 47 to control timing of operations throughout the memory system 40. Additionally, the memory controller 42 transfers data to and from the memory devices on a data bus 48. To control timing of data transfers to the memory device 44, the memory controller 42 provides a data clock signal DCLK on a data clock bus 50. The data clock signal DCLK forms a clocking signal that indicates arrival of the data DAT at each of the memory devices 44.

The master clock signal MCLK is a continuously running clock that provides overall system timing while the data clock DCLK is discontinuous, *i.e.*, the data clock signal DCLK contains clock pulses only during intervals in which write data DAT is present.

Upon initialization of the memory system 40, the memory controller 42 establishes the timing of each of the memory devices 44 such that data DAT from the memory devices 44 arrive at the memory controller 42 coincident with edges the master clock signal MCLK as will now be described.

To establish the timing, the memory controller 42 first sends control data packets to each memory device 44 instructing the memory devices 44 to provide selected data on the data bus 48 at specified edges of the master clock signal MCLK. With further reference to Figure 2, when the control data CDAT arrives at the memory device 44, the packet is captured in control data latches 54 in response to a delayed master clock signal CCLKD which is a phase-delayed version of the master clock signal MCLK. The delayed master clock signal CCLKD is produced by a delay-locked loop 58 as described in concurrently filed U.S. Patent Application Serial No. 5,920,518 ~~__________~~, entitled SYNCHRONOUS CLOCK GENERATOR INCLUDING DELAY-LOCKED LOOP which is commonly assigned herewith and which is incorporated herein by reference. The latched control data CDAT is then decoded by a logic control circuit 56 that controls operations within the memory device 44. The logic control circuit 56 identifies control data CDAT in the packet specifying a read operation and activates an I/O interface 62 to read data DAT from a memory array 64. The data DAT read from the memory array 64 are transferred to an output data latch 66 and then to a read FIFO register 94. The data DAT are held in the FIFO register 94 until the FIFO register 94 is activated by a delayed output clock signal DCLKO from coarse and fine verniers 95, 96. Initially (*i.e.*, prior to receipt of the packets of control data), the logic control circuit 56 sets the coarse and fine verniers 95, 96 with a default delay relative to the delayed master clock signal CCLKD to produce a delayed output clock signal DCLKO. The delayed output clock signal DCLKO activates the read FIFO register 94 to place the output data DAT on the data bus 48.

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The memory controller 42 receives the data from the data bus 48 and compares the arrival times of the data to the specified edges of the master clock signal MCLK. Based upon the comparisons, the memory controller 42 determines respective routing delays for each of the memory devices 44 and issues a second control data packet to each of the memory devices 44 establishing an internal timing adjustment to compensate for the respective routing delay. The memory device 44 receives the second control data packet and the logic control circuit 56 identifies control data CDAT within the packet specifying a coarse delay adjust and a fine delay adjust and outputs coarse and fine adjust signals ADJ_C, ADJ_F, thereby adjusting the coarse and fine verniers 95, 96 to compensate for the routing delays.

While the above approach allows control of the initial delay in each of the memory devices 44 upon initialization of the memory system 40, the initial settings of the coarse and fine verniers 95, 96 may become incorrect if the routing delays of the data clock bus 50 or the master clock bus 47 drift over time, as for example, may be caused by aging, temperature or frequency variations. Consequently, the timing of the memory system 40 may no longer be such that the data DAT arrive at the memory controller 42 coincident with edges of the master clock signal MCLK. Under such circumstances, some data may be lost, or the memory system 40 may not operate at its optimum rate.

Figure 3 shows a memory system 80 according to another embodiment of the invention that corrects drifts of the signal timing. The memory system 80 operates under control of a memory controller 82 that controls eight memory devices 84 through commands issued over the control data bus 46 and through the master clock signal MCLK carried by the master clock bus 47. Additionally, the memory controller 82 transmits data to and receives data from the memory devices 84 over the data bus 48 and provides the data clock signal DCLK synchronously with the data DAT to enable latching of the data DAT at the memory devices 84.

Figure 4 shows the structure of one of the memory devices 84 in greater detail in which the memory device 84 receives control data CDAT at the control data latches 54. The latches 54 latch the control data CDAT in response to the delayed master clock CCLKD produced by the delay-locked loop 58.

When the memory controller 82 instructs the memory device 44 to output data, the logic control circuit 56 activates the I/O interface 62 to transfer data from the memory array 64 to the output FIFO 94. The data DAT are held in the FIFO register 94 until the delayed output clock signal DCLKO activates the FIFO register 94.

As with the memory device 84 discussed previously, the coarse and fine verniers 96 provide the delayed output data clock signal DCLKO in response to the delayed master clock signal CCLKD. The fine vernier 96 is a variable delay line having its delay time controlled by the logic control circuit 56. The fine vernier 96 is selectively adjustable to adjust the delay between the delayed master clock signal CCLKD and the delayed output clock signal DCLKO by increments of approximately 150 ps. The fine vernier 96 therefore activates the FIFO register 94 to transmit the read data before or after the specified leading edge of the master clock MCLK. As discussed previously, the fine vernier 96 thus allows each memory device 84 to be "tuned" to compensate for routing delay differences between various memory devices 84 and the memory controller 82.

Unlike the previously described embodiment, the memory device 84 of Figure 4 also provides the delayed output data clock signal DCLKO to the data clock bus 50 as an echo clock signal ECHOCLK. The echo clock signal ECHOCLK travels to the memory controller 82 on the data clock bus 50 coincident with the output data DAT traveling on the data bus 48. The propagation times of signals on the data clock bus 50 and the data bus 48 are substantially the same. Therefore, drifts in the timing of echo clock signal ECHOCLK timing will mirror drifts in timing of the data DAT. The memory

controller 82 can thus continuously monitor and correct variations in routing delays, as will be described now with reference to Figure 5.

As shown in Figure 5, the memory controller 82 receives the echo clock signal ECHOCLK from the data clock bus 50. Within the memory controller 82, the echo clock signal ECHOCLK is applied to respective first inputs of five phase comparators 102. The second inputs of the phase comparators 102 are driven by respective outputs of a multiple output delay-locked loop 104 driven by the master clock signal MCLK. The delay-locked loop 104 provides phase-shifted output signals at the frequency of the master clock signal MCLK with respective positive or negative phase shifts relative to the master clock signal MCLK. Each of the phase comparators 102 compares the echo clock signal ECHOCLK to the respective output of the delay-locked loop and outputs a respective phase compare signal ϕ_1-ϕ_5. A phase logic circuit 108 receives the phase signals ϕ_1-ϕ_5 and identifies the approximate phase shift of the echo clock signal ECHOCLK relative to the master clock signal MCLK by comparing the phase signals ϕ_1-ϕ_5. The phase logic circuit 108 then provides phase error signals ϕ_{ERROR} to a logic control circuit 110 indicating the phase shift and other conditions, including the direction of the phase shift.

The logic control circuit 110 uses the phase error signals ϕ_{ERROR} to determine whether or not the echo clock signal ECHOCLK is within one vernier increment of the master clock signal MCLK. If the echo clock signal ECHOCLK is not within one vernier increment of the master clock signal MCLK, the logic control circuit 110 sends control data (in the next set of control data addressed to the memory device 84) to command the memory device 84 to adjust the vernier by one or more increments. In response to the control data from the memory controller 82, the logic control circuit 56 (Figure 4) establishes a new fine adjust signal ADJ_F to adjust the setting of the fine vernier 96 (Figure 4). The delay of the fine vernier 96 changes the delay of the delayed output clock signal DCLKO

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correspondingly. Because the delayed output clock signal DCLKO controls timing of data DAT on the data bus 48, the revised output data signal DCLKO changes the timing of data DAT as instructed by the memory controller 82. The memory controller 82 thus continuously monitors and corrects the timing of the memory devices 84 such that the data DAT arrive at the memory controller 82 coincident with edges of the master clock signal MCLK.

Figure 6 is a block diagram of a computer system 200 that contains the memory controller 82 of Figure 5 and three of the memory devices 84 of Figure 4. The computer system 200 includes a processor 202 for performing computer functions such as executing software to perform desired calculations and tasks. The processor 202 also includes command, address and data buses 210 to activate the memory controller 82, thereby controlling reading from and writing to the memory devices 84. One or more input devices 204, such as a keypad or a mouse, are coupled to the processor 202 and allow an operator to manually input data thereto. One or more output devices 206 are coupled to the processor 202 to display or otherwise output data generated by the processor 202. Examples of output devices include a printer and a video display unit. One or more data storage devices 208 are coupled to the processor to store data on or retrieve data from external storage media (not shown). Examples of storage devices 208 and storage media include drives that accept hard and floppy disks, tape cassettes and compact-disk read-only memories.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. For example, the echo clock signal ECHOCLK may be carried by a separate signal line, rather than being carried by the data clock bus 50. Similarly, the memory controller 82 can employ other phase comparing circuits in place of the delay-locked loop 104 and bank of phase comparators 102. Also, although the embodiment described herein adjusts both the coarse

and fine verniers 95, 96, where the drift of timing in not excessive, the memory controller 42 may transmit data adjusting only the fine vernier 96. In such an embodiment, the logic control circuit 56 keeps track of the total phase shift of the fine vernier 96 so that, if the fine vernier 96 reaches its adjustment limit or would move the phase shift past 360°, the logic control circuit 56 increments the coarse vernier 95 by one clock period and returns the fine vernier 95 to a lower setting referenced to the new course vernier setting. Accordingly, the invention is not limited except as by the appended claims.